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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,101	01/15/2002	Toshinori Goto	MAE 251	1247
23995	7590	11/16/2004	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			PAN, DANIEL H	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/045,101

Applicant(s)

GOTO, TOSHINORI

Examiner

Daniel Pan

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-8 is/are rejected.
- 7) ☒ Claim(s) 4,9 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

1. Claims 1-10 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1,2, 5, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (5,925,139) in view of Raz (5,701, 480).

3. As to claim 1, 5, Yamada disclosed a microcontroller system (see fig.1) comprising at least :

- a) a central processing unit [CPU] for executing program to activate a halt signal to stop execution of program (see fig.1, see the executing inhibiting by means of the stopping clock in col.4, lines 30-43) ;

- b) a memory storing data including program (see the EEPROM in fig.1), receiving a mode for outputting (reading) data and discontinuing the outputting based on the mode activation states (see the mode for reading in col.4, lines 13-16, 57-62, col.6, lines 4-6);

- c) when a halt was activated (see the high level of select) , reading certain part of the memory (see the reading of the command in col.4, lines 57-67);

- d) supplying the central processing unit with the stored part of program (see the reading of the command in col.4, lines 57-67).

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4. Yamada did not specifically show the activation of the halt signal to stop the execution of program until an interrupt was received as claimed. However, Raz disclosed a system for including an interrupt to clear a halt signal (see the clear of inhibit flag in col.19, lines 34-49) . It would have been obvious to one of ordinary skill in the art to use Raz in Yamada for including the interrupt for inactivate the halt as claimed because the use of Raz could provide the control ability to accept specific transactions, or tasks (e.g. memory access, or read/write requests) at a predefined processing stage, such as the restoration or resume execution cycle, for the continuing processing, and therefore, enhancing the processing capability to adapt to exception conditions (e.g. interrupts, due to hazard, or abnormal events) of the system, and it could be achieved by configuring the interrupt routine of Raz with modified control parameters (e.g. the interrupt clock) into Yamada so the interrupt signal of Raz could be recognized by Yamada in order to provide the resume control the program, and for the above reasons, provided a motivation.

5. As to claim 2, Yamada did not specifically show the latches for storing the part of program as claimed. However, Yamada, in the same patent, disclosed that part of the program (the respective program commands) was received by a DOUT output terminal, and that the CPU latched the data address with the clock (see col.6, lines 38-43) , therefore, a latch, or the like, had to be included in order to stabilize the input at CPU during the clock period.

6. As to claim 8, Yamada also included ready signal for memory output (see the MODE set for reading out from memory in col.4, lines 57-62).

7. Claims 3, 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (5,925,139 in view of Raz) (5,701, 480) as applied to claims 1, 5 above, and further in view of Swoboda et al. (5,564,028).

8. As to claim 3, neither Yamada nor Raz specifically showed the FIFO as claimed. However Swoboda disclosed FIFO see col.10, lines 45-48). It would have been obvious to one of ordinary skill in the art to use Swoboda in Yamada for including a FIFO as claimed because the use of Swoboda could provide the additional type of the storage capability into Yamada, and because Yamada did disclose subsequent commands at corresponding

CPU execution time slot (see fig.4), therefore, one of ordinary skill in the art should be able to recognize the need of a specific format of storage, such as FIFO, in CPU to keep the proper order of the execution time.

9. As to claims 6, 7, neither Yamada nor Raz specifically showed the counter for the interrupt as claimed. However, Swoboda disclosed a counter for delaying an interrupt (see col.11, lines 4-16). It would have been obvious to one of ordinary skill in the art to use Swoboda in Yamada for including an interrupt counter as claimed because the use of Swoboda could provide Yamada the ability of resuming the processing at a predefined level in a given interrupt command, thereby providing the recoverable control of the program sequence.

10. Claims 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further recites the selections of the first address signals when the halt was in the respective active and inactive states.

11. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the flip-flop delaying signal from the memory, the inverter, the logic gate passing the interrupt to the central processing unit, receiving the interrupt, the delaying signal and the inverted signal.

12. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the flip-flop generating the mode signal set by halt and reset by interrupt.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Gerchman et al. (6,334,167) is cited for the teaching of the activation of the read and write control mode of the access to memory (see col.2, lines 51-67, col.3, lines 1-14).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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GROUP